February 9, 2012

DS30BA101

3.125 Gbps Differential Buffer

General Description

The DS30BA101 is a high-speed differential buffer for cable driving, signal buffering, and signal repeating applications. Its fully differential signal path ensures exceptional signal integrity and noise immunity. The DS30BA101 drives both differential and single-ended transmission lines at data rates up to 3.125 Gbps.

The output voltage amplitude is adjustable via a single external resistor for cable driving applications into 75Ω single-ended and 100Ω differential mode impedances.

The DS30BA101 is powered from a single 3.3V supply and consumes 165 mW (typical). It operates over the full industrial temperature range of -40°C to +85°C and is available in a 4 x 4 mm 16-pin LLP package.

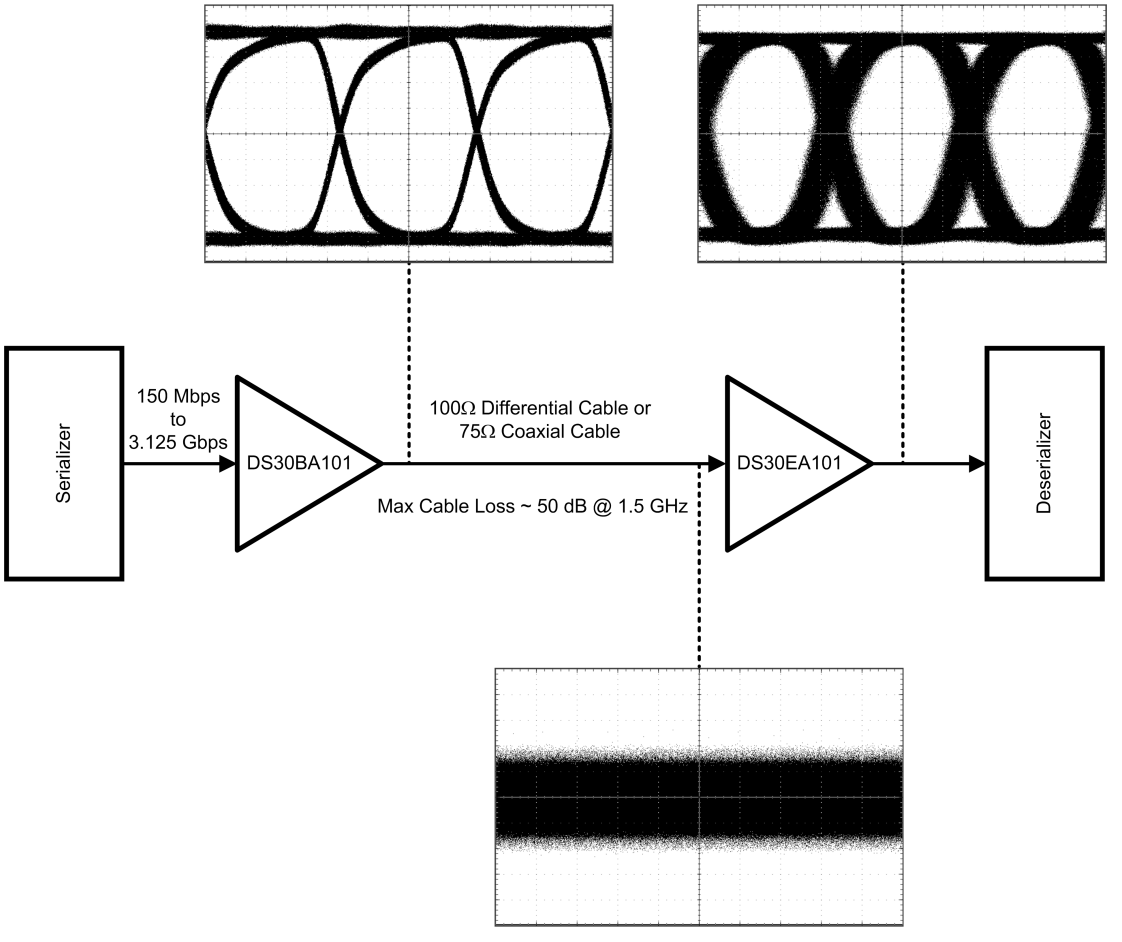
Features

- Data rates from DC to 3.125 Gbps
- Supports SD and HD video resolutions
- Power consumption: 165 mW typical
- Industrial temperature range: -40°C to +85°C

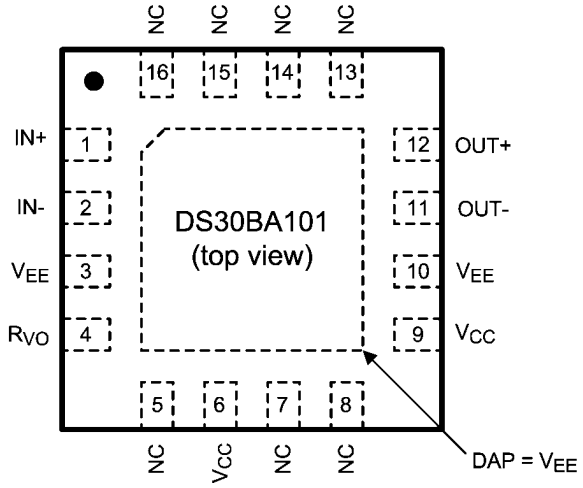
Applications

- Cable extension
- Signal buffering and repeating
- Security and surveillance

Typical Application



Connection Diagram



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The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

16-Pin LLP
Order Number DS30BA101SQ
Package Number SQB16A

Ordering Information

Part Number	Package	Quantity
DS30BA101SQ	16-Pin LLP, 4.0 x 4.0 x 0.8 mm, 0.65 mm pitch	Reel of 1000
DS30BA101SQE	16-Pin LLP, 4.0 x 4.0 x 0.8 mm, 0.65 mm pitch	Reel of 250
DS30BA101SQX	16-Pin LLP, 4.0 x 4.0 x 0.8 mm, 0.65 mm pitch	Reel of 4500

Pin Descriptions

Pin	Name	I/O, Type	Description
1	IN+	I, CML	Non-inverting input.
2	IN-	I, CML	Inverting input.
3	V_{EE}	Ground	Negative power supply (ground).
4	R_{VO}	I, Analog	Output voltage level control. Connect a resistor between this pin and V_{CC} to set the output voltage.
5	NC	N/A	No connect. Not bonded internally.
6	V_{CC}	Power	Positive power supply (+3.3V).
7	NC	N/A	No connect. Not bonded internally.
8	NC	N/A	No connect. Not bonded internally.
9	V_{CC}	Power	Positive power supply (+3.3V).
10	V_{EE}	Ground	Negative power supply (ground).
11	OUT-	O, Data	Inverting output.
12	OUT+	O, Data	Non-inverting output.
13	NC	N/A	No connect. Not bonded internally.
14	NC	N/A	No connect. Not bonded internally.
15	NC	N/A	No connect. Not bonded internally.
16	NC	N/A	No connect. Not bonded internally.
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Absolute Maximum Ratings (Note 1)

Supply Voltage:	3.6V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Output Current	28 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance	
θ_{JA} 16-pin LLP	+58°C/W
θ_{JC} 16-pin LLP	+21°C/W
ESD Rating (HBM)	≥±4.5 kV
ESD Rating (MM)	≥±250V
ESD Rating (CDM)	≥±2 kV

Recommended Operating Conditions

Supply Voltage (V_{CC}):	3.3V ±5%
Operating Free Air Temperature (T_A)	-40°C to +85°C

DC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 2, Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{ICM}	Input Common Mode Voltage		IN+, IN-	1.1 + V_{ID}/2		V_{CC} − V_{ID}/2	V
V_{ID}	Input Voltage Swing	Differential		100		2200	mV_{P-P}
V_{OCM}	Output Common Mode Voltage		OUT+, OUT-		V_{CC} − V_{OUT}		V
V_{OUT}	Output Voltage	Single-ended, 75Ω load, R_{VO} = 750Ω			800		mV_{P-P}
		Single-ended, 50Ω load, R_{VO} = 953Ω			400		mV_{P-P}
I_{CC}	Supply Current				50	59	mA

AC Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 2, Note 3)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{IN}	Input Data Rate		IN+, IN-			3125	Mbps
t_{TLH}	Transition Time Low to High	20% - 80% (Note 4)	OU++, OUT-		90	130	ps
t_{THL}	Transition Time High to Low				90	130	ps

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device my occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: Typical values represent most likely parametric norms at V_{CC} = +3.3V, T_A = +25°C, and at the Recommended Operating Conditions at the time of product characterization and are not guaranteed.

Note 4: Specification is guaranteed by characterization and is not tested in production.

Device Operation

INPUT INTERFACING

The DS30BA101 accepts either differential or single-ended input. DC-coupled inputs must be kept within the specified common-mode range.

OUTPUT INTERFACING

The DS30BA101 uses current mode outputs. Single-ended output levels are 800 mV_{P-P} into 75Ω AC-coupled coaxial cable with an R_{VO} resistor of 750Ω, or 400 mV_{P-P} (800 mV_{P-P} differential) into 100Ω differential cable with an R_{VO} resistor of 953Ω. The output voltage level is controlled by the value of the R_{VO} resistor connected between the R_{VO} pin and V_{CC}.

The R_{VO} resistor should be placed as close as possible to the R_{VO} pin. In addition, the copper in the plane layers below the R_{VO} network should be removed to minimize parasitic capacitance.

Figure 1 and *Figure 2* show the typical configurations for differential output and single-ended output, respectively. For single-ended output, the unused output must be properly terminated as shown.

Application Information

CABLE EXTENDER APPLICATION

The DS30BA101 together with the DS30EA101 form a cable extender chipset optimized for extending serial data streams from serializer/deserializer (SerDes) pairs and FPGAs over 100Ω differential cables and 75Ω coaxial cables. Setting the correct DS30BA101 output amplitude and proper cable termination are essential for optimal operation. *Figure 1* shows the recommended chipset configuration for 100Ω differential cable and *Figure 2* shows the recommended chipset configuration for 75Ω coaxial cable.

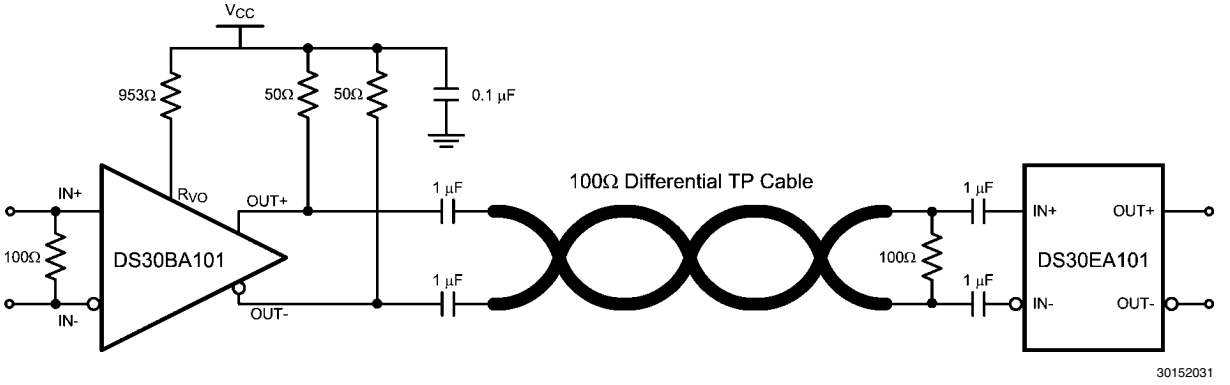


FIGURE 1. Cable Extender Chipset Application Circuit for 100Ω Differential Cable

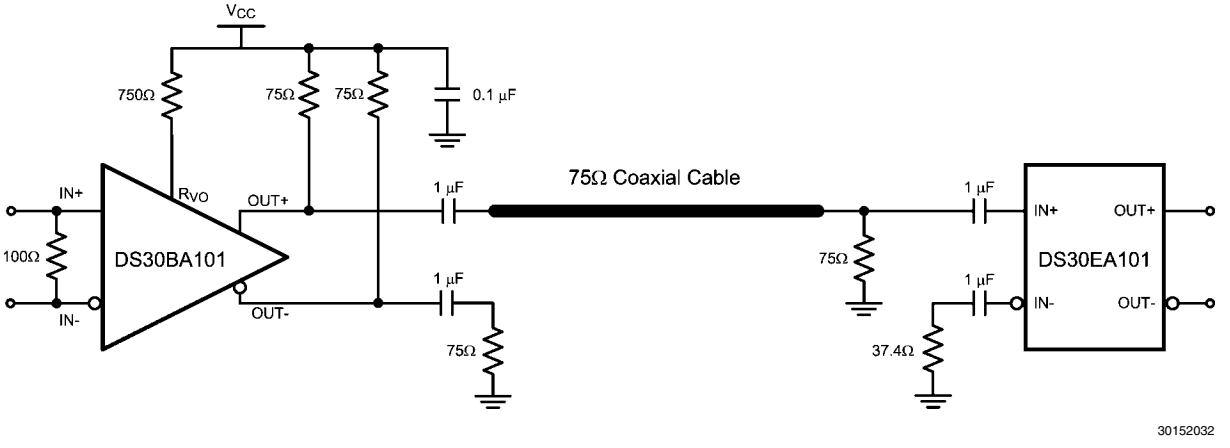
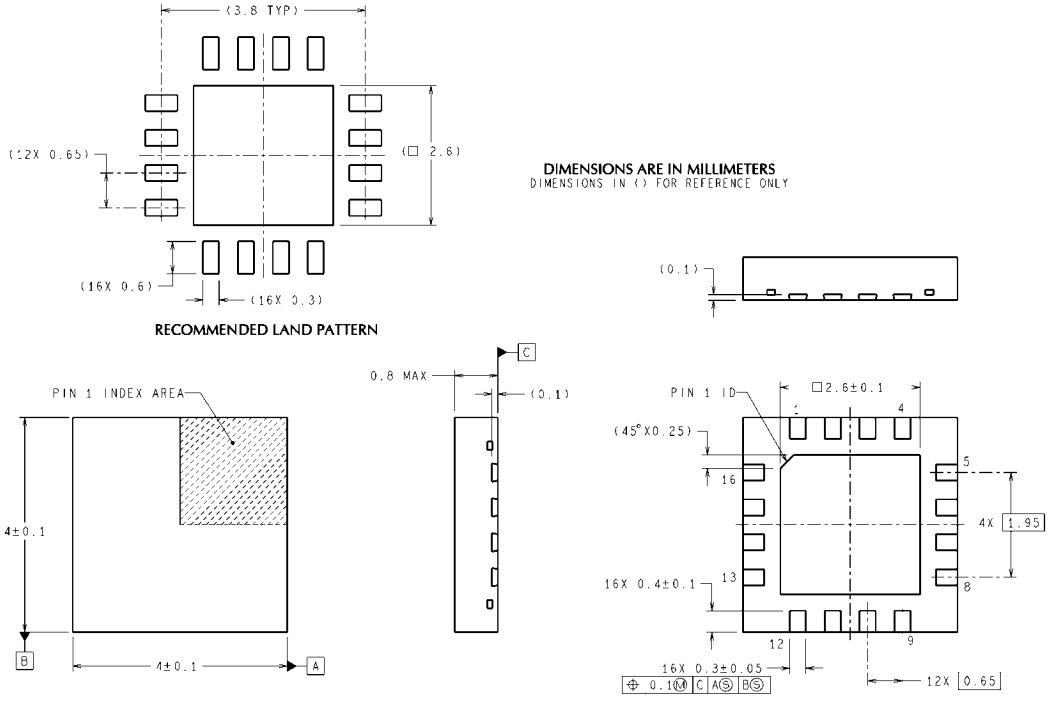


FIGURE 2. Cable Extender Chipset Application Circuit for 75Ω Coaxial Cable

Physical Dimensions inches (millimeters) unless otherwise noted



SQB16A (Rev A)

16-Pin LLP
Order Number DS30BA101SQ
Package Number SQB16A

Notes

Notes

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